A Transferred-Substrate HBT Wide-Band Differential Amplifier to 50 GHz

B. Agarwal, Q. Lee, R. Pullela, D. Mensa, J. Guthrie, and M. J. W. Rodwell

***Abstract*— Differential amplifiers are used in automatic gain control amplifiers and limiting amplifiers in fiber-optic receivers. Here we present a differential amplifier fabricated in the transferred-substrate heterojunction bipolar transistor (HBT) integrated circuit technology. The amplifier has a gain of 11 dB and the 3-dB bandwidth is greater than 50 GHz. Two gain stages with dc interstage coupling are used. Biasing is through active current mirrors and a single negative power supply. A bandwidth of 50 GHz is the highest bandwidth ever reported for a broad-band differential amplifier in any technology.**

***Index Terms*—Broad band, differential, HBT, InP, transferred-substrate.**

I. Introduction

BROAD-BAND amplifiers are key components in fiber-optic receivers [1]–[6]. They are used in the main amplifier to amplify the weak signals received from the preamplifier. The output amplitude of the main amplifier must be constant irrespective of the wide input dynamic range, thus requiring a automatic gain control (AGC)-type or a symmetric limiting-type amplifier. Limiting amplifiers are also used in the clock recovery circuit to provide a constant amplitude recovered clock. Apart from keeping the output level constant, the main amplifier must have high broad-band gain, flat gain characteristics from dc to ~70% of the bitrate and constant group delay. Often, a differential amplifying stage forms the core in such amplifiers. The advantages of differential operation compared to single-ended operation are improved immunity to electromagnetic crosstalk, good common mode suppression, ease of dc biasing, and symmetric nonsaturating limiting characteristics. The amplifiers could be implemented in either lumped or distributed configuration. Distributed amplifiers generally obtain a higher bandwidth in a given transistor technology. However, good low-frequency response is difficult to achieve, in-band gain ripple is often present, and die areas are large. Lumped amplifiers can be dc-coupled, and have smaller die areas and smooth gain–frequency characteristics. The bandwidth of amplifiers reported in literature is often limited either by intrinsic device bandwidth or by technological limitations (like poor heat-sinking or wiring capacitance) or a combination of both. Future high-speed fiber-optic systems will require amplifiers with very high bandwidths.

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The authors are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA.

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This letter presents a broad-band lumped differential amplifier in the AlInAs/GaInAs transferred-substrate HBT IC technology. This technology has demonstrated devices with >400-GHz bandwidth [7], and resistive feedback amplifiers with 50-GHz bandwidth [8]. Here we present a two-stage dc-coupled differential amplifier. The low-frequency gain is 11 dB and the 3-dB bandwidth is greater than 50 GHz. Biasing is done with active heterojunction bipolar transistor (HBT) current mirrors and a single negative power supply. A bandwidth of 50 GHz is the highest bandwidth ever reported for a broad-band differential amplifier in any technology.

II. Technology

The epitaxial layer structure and fabrication process is described in our earlier work [7]. Fig. 1 shows a schematic cross section of the IC process. Devices with emitter dimensions of 0.75×25 μm^2 and collector dimensions of about 1.8×29 μm^2 were fabricated on this wafer. From dc common-emitter characteristics, the small-signal current gain at dc, β, is 50. BV_{CEO} is about 3 V, but reduces to 1.5 V at 10^5 A/cm^2. BV_{CBO} is 6 V. From the measured current gain and the unilateral power gain versus frequency, the extrapolated f_τ and $f_{\max}$ are 160 and 370 GHz, respectively. Fig. 2(a) and (b) shows variation of f_τ and $f_{\max}$ with emitter current density J_E and collector–emitter voltage V_{CE}, respectively. Peak f_τ is 175 GHz and is obtained at $J_E = 1.6 \times 10^5$ A/cm^2 and $V_{CE} = 1$ V. Peak $f_{\max}$ is 370 GHz at $J_E = 1.0 \times 10^5$ A/cm^2 and $V_{CE} = 1.1$ V. The amplifier is designed to operate close to peak f_τ and $f_{\max}$ bias.

III. Circuit Design

Fig. 3 shows a schematic circuit diagram of the amplifier with the element values. A variation of the classic transadmittance-transimpedance design by Cherry and Hooper [9] with 50-Ω interstage impedances is used here. The first stage has a emitter-coupled pair with input emitter follower buffers and emitter degeneration. 50-Ω shunt input resistors set the input impedance of the overall amplifier. 50-Ω output resistors are used in the collectors, setting a 50-Ω output impedance of the first stage. The second stage employs transimpedance loading to obtain a 50-Ω input impedance and 50-Ω output impedance. Level-shifting diodes are used to bias all transistors below breakdown. Active biasing with transistor current mirrors and a single negative supply is used. Input and output dc levels are designed to be the same thus enabling dc coupling between successive stages of the

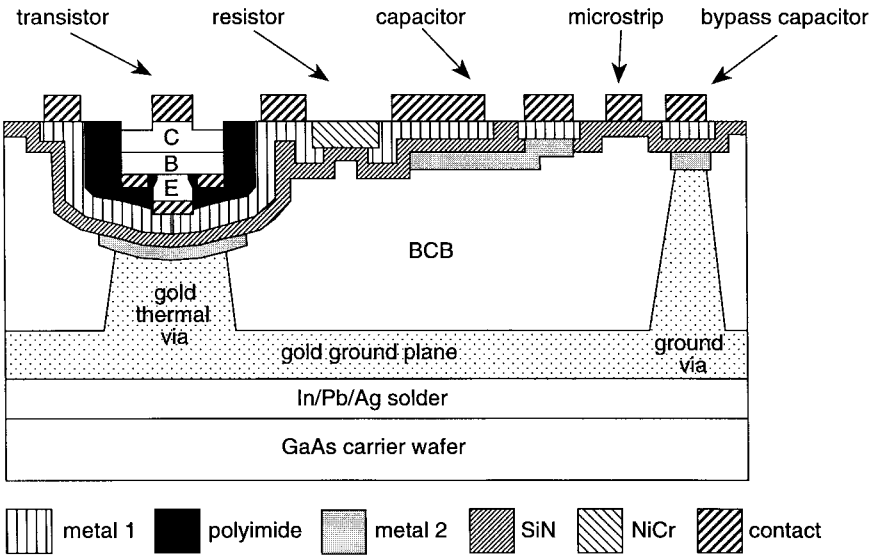

Fig. 1. Schematic cross section of the IC fabrication process.

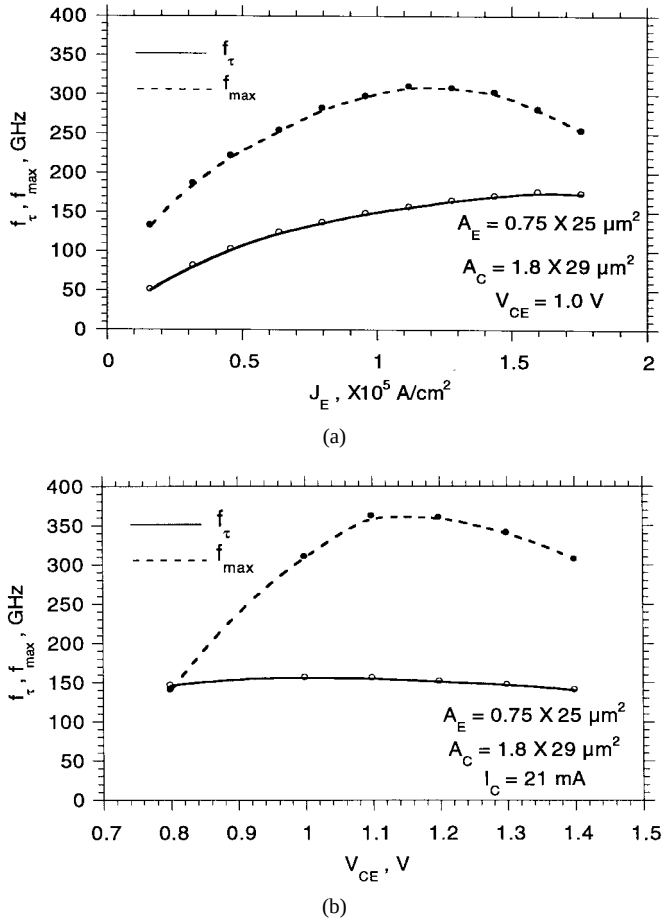

Fig. 2. Variation of f_τ and $f_{\max}$ with (a) emitter current density J_E and (b) collector–emitter voltage V_{CE}.

amplifier. Fig. 4 shows a photomicrograph of the amplifier. A total of 22 transistors are used. The chip dimensions are 0.75 mm $\times$ 0.44 mm.

IV. Results

The amplifier performance was measured with a network analyzer from 45 MHz to 50 GHz. Only single-ended characteristics (two-port) were measured, with the other ports terminated off-chip in 50 Ω. The negative supply was at -2.5 V and the input dc level of -0.3 V was applied with a independent supply. The total bias current through the amplifier was 96 mA. The IC consumes 250-mW dc power. Fig. 5 shows the forward gain s_{21} of the amplifier. The low-frequency gain is 11 dB and the 3-dB bandwidth is $>$50 GHz. The dashed curve shows the gain of a different amplifier at different bias conditions. A lower bandwidth and a more flat response is obtained. The bias voltages and overall current is the same, but the reference current in the first gain stage is reduced (from 14 to 11 mA) and that of the second gain stage is increased. The low-frequency gain is the same, but the in-band gain variation is less than 1 dB, and the bandwidth is 40 GHz for the dashed curve. Such flat gain response is important for acceptable bit error rates in high-speed systems. The gain ripple at high frequencies is a result of using a two-port calibration with off-chip terminations of the two unused ports. Fig. 6 shows the input and output return losses and the reverse isolation of the amplifier.

V. Conclusions

We have demonstrated a broad-band dc-coupled differential amplifier with AlInAs/GaInAs transferred-substrate HBT's. The amplifier achieves 11-dB gain and $>$50-GHz 3-dB bandwidth. A bandwidth of 50 GHz is the highest bandwidth ever reported for a broad-band differential amplifier in any technology. Higher device bandwidths, and hence higher circuit bandwidths, are possible by scaling the emitters and collectors of transferred-substrate HBT's to submicron dimensions. Variable-gain operation is possible in this configuration by varying the emitter currents of the emitter-coupled pair in the first stage. This will be addressed in future more sophisticated designs. The use of a microstrip wiring environment, along with low-inductance ground vias and a ground plane, make IC's in this technology suitable for packaging. Amplifiers with these high bandwidths will be useful for future high-speed communication systems.

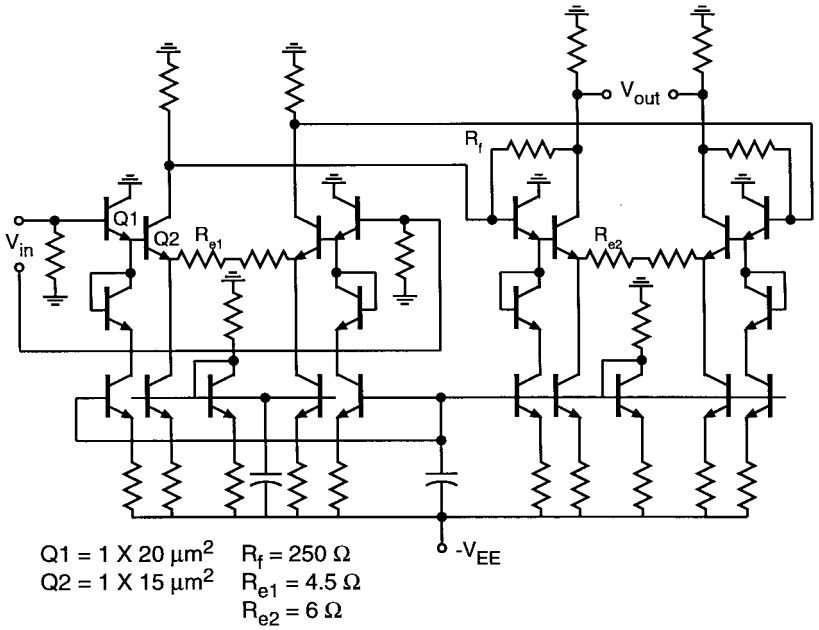

Fig. 3. Schematic circuit diagram of the amplifier.

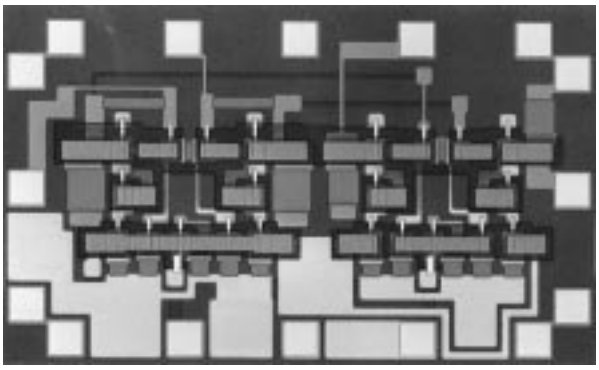

Fig. 4. Photograph of the differential amplifier IC (0.75 mm × 0.44 mm).

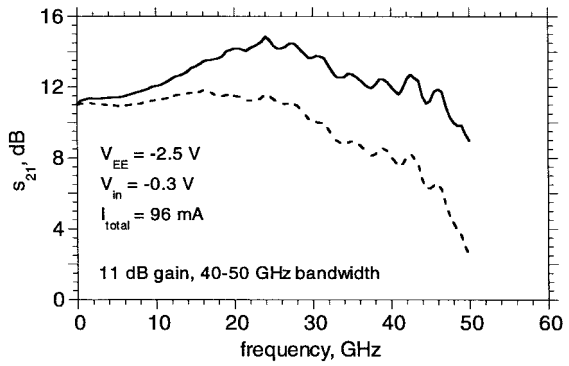

Fig. 5. Measured forward gain s_{21} of the amplifier.

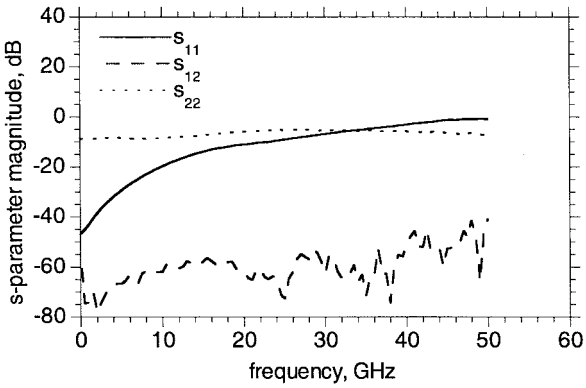

Fig. 6. Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

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